IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Yasukiyasu Sugano et al.

Confirmation No. 2204

Application No.: 09/478,812

Group Art Unit: 2815

Filed: January 7, 2000

Examiner: Eugene Lee

For: PROCESS FOR PRODUCING THIN FILM SEMICONDUCTORDEVICE AND LASER IRRADIATION APPARATUS

APPELLANT'S REVISED BRIEF RESPONSIVE TO NNC

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This revised and restated brief is a revised Appeal Brief under 37 C.F.R. §41.37 appealing the final decision of the Examiner dated August 28, 2006. Each of the topics required by 37 C.F.R. §41.37 is presented herewith and is labeled appropriately. A Notice of Appeal was filed on January 26, 2006 with a request for an extension of time for two months. This Appeal Brief was accompanied by a request for an extension of time for three months to file this appeal brief. Thus, this submission was timely.

Response to Notice of Non-Compliant Appeal Brief

This revised and restated Brief on Appeal is responsive to the Notice of Non-Compliant Appeal Brief of July 27, 2007 and is accompanied by a request for an extension of time for five (5) additional months. Thus, this submission is timely and responsive to the Notice of Non-Compliant Appeal Brief. In this paper, the alleged "Improper Headings" are changed so that "Issues" are renamed as –Grounds of Rejection to be Reviewed--, and "Grouping of Claims" as

originally presented is re-presented in the Arguments. These points are responsive to section 10.1 in the Notice of Non-Compliant Brief.

In addition, it should be noted that none of the independent claims here on appeal contains "means" clauses. Thus, the requirements of section 4(b)(1) and 4(b)(2) are not applicable. As to the alleged deficiencies in section 4(a), the original summary of invention section provided a concise explanation of the subject matter defined in the independent claims on appeal. Thus, this requirement is respectfully traversed, particularly since: (1) the essence of the claims on appeal were considered in a prior appeal (see Judge Saadat's earlier opinion discussing representative claim 11); and (2) the sole issue on appeal for consideration is whether it was appropriate for the examiner to ignore certain terminal language in each of the independent claims as involving "product by process". No issue is advanced as to the impropriety of the omission of consideration if the alleged product by process language is properly fully neglected.

The Notification also suggests that each independent claim be mapped to the specification by page and line number; such mapping is not necessary in view of the issues on appeal relating solely to the neglect of certain language when considering an application of the art – the very language relied upon by the Applicant is overcoming the applied art. Nevertheless, the salient portions of the independent claims are better tied to the discussion for the convenience of the Board.

Judicial economy would suggest that a lengthy claim chart mapping the claims to the specification for this appeal and its narrow scope is not necessary.

Background Discussion

This application relates to a process for producing a thin film semiconductor device and a laser irradiation apparatus. While this application has had a long and difficult prosecution, its divisional applications were favorably received. Thus, its first divisional application, Application No. 09/731,905 filed on December 8, 2000 was issued on October 14, 2003 as U.S. Pat. No. 6,632,711. Its second divisional application, Application No. 010/061,392, filed on February 4, 2002 was issued on February 17, 2004 as U.S. Pat. No. 6,693,258. Copies of those two patents are appended to this Brief for the information of the Board when considering the issues in this Appeal. The method claims in those two divisional applications contain function language equivalent to the apparatus language presented for consideration here.

It is believed that **no additional fees other than the extension fees are due**. M.P.E.P. §1208.03. However, if a fee is required, the Commissioner is hereby authorized to charge the fee to Deposit Account # 18-0013 and refer to SON-1718.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventors and recorded by the U.S. Patent and Trademark Office at reel 010792, frame 0182.

II. RELATED APPEALS AND INTERFERENCES

There are no other pending appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal of which the Appellants are aware. A prior related Decision on Appeal rendered in this application on June 30, 2004 (copy included in the Related Appeals Appendix) affirmed the rejection of the examiner and resulted in an RCE filed on August 30, 2004.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 14 claims pending in application, i.e. pending claims 11, 12, 17, 18, 27, 28, 39, 40, 53, 54, 63, 65, 73, and 74, of which each is an independent claim.

B. Current Status of Claims

The Application as filed contained claims 1 to 74. After canceling claims in view of a restriction requirement and other subsequent actions and amendments, only claims 11 to 12, 17 to 18, 27 to 28, 39 to 40, 53 to 54, 63, 65, and 73 to 74 are pending on appeal. No amendments have been made to the claims since the mailing of the Final Action of August 28, 2006 except for a deletion of a duplicative use of "wherein" in pending claim 11 to overcome an objection of the examiner; that change was made in the pending claims because of its non-controversial nature to satisfy an examiner requirement.

1. Claims canceled: 1-10, 13-16, 19-26, 29-38, 41-52, 55-62, 64 and 66-72
2. Claims withdrawn from consideration but not canceled: None
3. Claims pending: 11, 12, 17, 18, 27, 28, 39, 40, 53, 54, 63, 65, 73, 74
4. Claims allowed: None
5. Claims rejected: 11, 12, 17, 18, 27, 28, 39, 40, 53, 54, 63, 65, 73, 74

C. Claims On Appeal

The claims on appeal are claims 11, 12, 17, 18, 27, 28, 39, 40, 53, 54, 63, 65, 73, 74

IV. STATUS OF AMENDMENTS

Claims 11 to 12, 17 to 18, 27 to 28, 39 to 40, 53 to 54, 63 to 65, and 73 to 74 were initially examined after the above-mentioned RCE. A non-final Action dated February 15, 2006 was issued, and a response dated June 15, 2006 containing the claims here on appeal (except for a minor amendment to claim 11 to overcome an objection at final action) was submitted. Following the Final Action, the Applicant's did not file a Response to Final Office Action, and

the Notice of Appeal was thereafter filed.

Thus, the claims as presented in the Appendix represent all amendments that were made up until issuance of the Final Action.

V. SUMMARY OF INVENTION

Each of the pending independent claims on appeal is clear in defining the pending invention for each claim. Specifically, each claim refers to a device, not a method.

Each of the independent claims refers to a thin film semiconductor device whether per se or as a component of a display device. For background, it can be noted for each independent claim that a first aspect of the present invention includes a thin film semiconductor device. The device includes a semiconductor thin film (e.g. layer 5, Fig. 7D), with a gate insulating film (combined film layers 2 and 3) accumulated on one surface thereof (lower surface of layer 5). A gate electrode (1) is accumulated on the semiconductor thin film (5) via the gate insulating thin film (2 and 3). The semiconductor thin film of each independent claim is formed by forming a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon (layer 4 in Fig. 7B, page 39, lines 13 to 15).

Each independent claim notes that the polycrystalline silicon is an irradiation converted substrate. An energy beam is applied to a prescribed region, and a cross sectional shape of the energy beam is adjusted with respect to the prescribed region to irradiate the prescribed region in a single shot (page 10, lines 14 to 19; page 39, line 23 to page 40, line 6).

As shown in Fig. 11, plural units may be formed on the substrate (0). In this case, the irradiation step is conducted so that the substrate (0) is irradiated intermittently in order to convert the amorphous or polycrystalline material (4) to a polycrystalline material (page 45, lines 6 to 19). Further, a cross sectional shape of the energy beam is adjusted with respect to each unit to irradiate one or two or more units at a time by a single shot irradiation (page 45, last line to page 46, line 3).

At the time of formation, the amorphous silicon or polycrystalline silicon (4) has a first particle diameter; and after being irradiated with the energy beam, the semiconductor thin film

(4) is converted to polycrystalline silicon (5) having a larger particle diameter than the first particle diameter (page 48, lines 10 to 16).

Regarding the laser irradiation step, such step may be performed by irradiating the prescribed region of the substrate one or more times with a pulse of laser light having a constant cross sectional area and an emission time width from upstand to downfall of 50 ns or more (Fig. 23A, page 69 lines 6 to 11). Further, a desired change to the energy intensity of the laser light from upstand to downfall of the pulse is applied to said polycrystalline silicon (page 67, line 16 to page 68, last line).

According to the first embodiment of the invention, a thin film transistor (112, Fig. 8) is integrated and formed in a prescribed region by using the semiconductor thin film (5) thus converted to polycrystalline silicon as an active layer (page 43, lines 13 to 17). Due to the energy beam irradiation, characteristics of the thin film transistor are made uniform.

A second aspect of the invention involves a display device as in claim 12 (Fig. 8, page 42, lines 12 to 15). The device includes a pair of substrates (101, 102) adhered to each other with a prescribed gap, and an electrooptical substance (103) maintained in the gap (page 42, lines 15 to 18). One of the substrates (102) includes a counter electrode, the other substrate (101) includes a pixel electrode (111) and a thin film transistor (112) driving the pixel electrode (111). The thin film transistor (112) includes a semiconductor thin film and a gate electrode accumulated on one surface of the semiconductor thin film through a gate insulating film as described above regarding the first aspect of the invention. The formation steps regarding the semiconductor thin film and the active region are also the same as described above.

A third aspect of the invention involves a thin film transistor having a laminated structure (Fig. 7, page 38, lines 17 to 19). The transistor includes a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated on said semiconductor thin film through said gate insulating thin film, according to the same construction as defined above regarding the first aspect of the invention. Further, the formation steps described above are the same, although in this embodiment, the semiconductor thin film is accumulated by alternately repeating the film forming step and the irradiation step, without exposing the substrate to the air (Fig. 14, page 52, lines 9 to 12).

A fourth aspect of the invention involves a display device as described above regarding the second aspect of the invention, using the method described above regarding the third aspect

of the invention. According to the principle of accumulation of the semiconductor thin film, a semiconductor thin film (2A in Fig. 19A to F) is formed by forming a layer of about 20 nm amorphous silicon or polycrystalline silicon having a first particle diameter on a substrate (page 59, lines 5 to 8). The film (2A) is irradiating according to a prescribed region of the substrate (1A) with laser light having a prescribed cross sectional shape to convert to polycrystalline silicon having a larger particle diameter than the first diameter as described above. Then, additional semiconductor thin films are accumulated by alternately repeating the film forming step, where each additional formed film is about 1 nm (page 60, lines 19 to page 61, line 4).

As stated above, with regard to any of the aspects of the invention, it is preferred that during the irradiation steps, the substrate is maintained in a non-oxidative atmosphere (page 27, lines 12 to 13). Further, in one embodiment it is preferred that the irradiation step is performed under conditions where the substrate is uniformly heated (page 26, lines 16 to 20). In another embodiment, the substrate is cooled to a temperature lower than room temperature during the irradiation step (page 26, line 24 to page 27, line 4).

The foregoing detailed discussion of the features of the invention can be distilled at this point to prepare for a discussion of the dispositive issues raised in the final Action. Specifically, the examiner in his final Action considered the following limitations in the claims as product by process limitations (see the Final Action, page 3, top, page 4, first full paragraph regarding claim 28, and supporting discussion at pages 6 and 7 of the Final Action.):

1. The limitation "wherein said semiconductor thin film is accumulated without exposing said substrate to the air" as stated in a terminal portion of each of the dependent claims;

2. The limitation "irradiated with pulse laser light having an emission time width from upstand to downfall of at least 50 ns"; and

3. The limitation "substrate is cooled to a temperature lower than room temperature".

VI. GROUNDS OF REJECTION TO BE REVIEWED

The issues presented for consideration in this appeal are as follows:

(1) Whether the Examiner erred in rejecting each of the pending claims 11, 23. 27. 18. 27, 28, 39, 40, 53, 54, 63, 65, 73, and 74 by failing to give ANY weight to the "accumulated without exposing the substrate to air" limitation under 35 U.S.C. §102(b) or §103 as stated in any of sections 3, 5, 6 and 7 of the Final Action.?

(2) Whether the Examiner erred in rejecting claim 39 under either sections 35 U.S.C. §102 or §103(a) as allegedly being unpatentable by failing to give ANY weight to the "pulse laser light" limitation?

(3) Whether the Examiner erred in rejecting claim 73 under either sections §102 or §103(a) by failing to give any weight to the "substrate is cooled limitation".

Each of these issues will be discussed in turn. Because of the framing of the issues in terms of the examiner's ignoring limitations specifically stated in the claims, and thus ignoring structural implications of the stated limitations, it is less important in this appeal to argue specifically the merits of each rejection if such limitations were fully considered since no such rejection was made. Furthermore, by holding for the Appellant as to the first issue, the case is disposed of until a rejection is rephrased to include the ignored limitation of the first issue. As to the second and third issues, only certain claims are disposed of until a rejection is rephrased to include the ignored limitations or either of them.

VII. ARGUMENTS, INCLUDING GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims are not grouped, but rather each of the inventions of each independent claims stands or falls separately in that at least one of its limitations has not been considered by the examiner.. The reasoning for the grouping of the claims is evident in light of the following arguments.

Introduction

For at least the following reasons, Appellant submits that these rejections are both technically and legally unsound and should therefore be reversed.

The claims that are pending for the Examiner's consideration in this application are apparatus claims that are directed to the thin film semiconductor devices that result from an inventive method. It is recognized that process limitations in product claims are not given any patentable weight **unless** they ascribe a structural feature to the resulting semiconductor chip. Therefore, the following discussion establishes how the process steps in the present claims do in

fact ascribe a structural feature to the semiconductors made thereby, which distinguish the semiconductors from those of the prior art.

While the following discussion emphasizes features of the claims that were ignored by the examiner as product by process limitations, it should be noted that each claim is a combination of features, including the features at issue, so that the structure of each claim can be considered in its entirety.

B. All Pending Claims Are Prima Facie Patentable Over the Applied Art When The Limitation "Accumulation Without Exposing the Film to Air" is Considered.

MPEP §2113 clearly suggests that the structure implied by process limitations should be considered when assessing the patentability of claims. Here, the terminal limitation of each of the pending claims on appeal refers to a film that is accumulated without exposing the substrate to air. Thus, a non-oxidized structure in the accumulated film thickness is implied and not shown in the art. See In re Garnero, 412 F. 2d 276, 279; 162 USPQ 221, 223 (CCPA 1979) discussed in MPEP §2113. Here, each of the inventions defined by each of the independent claims defines a structure having a particular characteristic, i.e. one that is implied by accumulation without exposing the substrate to air.

The only argument advanced by the examiner is that "such a process, as stated in the applicant's claims, does not structurally differentiate the thin film of Noguchi from the thin film in the Applicant's claims". This finding is respectfully traversed in that nothing in Noguchi suggests that his thin film is accumulated without exposing the substrate to air, as limited in each of the pending claims, see page 6 of the Final Action. In contrast, according to the specification at pages 51 et seq. and Fig. 14, the film forming step and the laser annealing step are alternately repeated to accumulate the semiconductor thin films without exposing the substrate to the air.

Why? By employing such a repeating process in vacuum (or inert gas) a step of removing contamination substances and dusts from the air can be eliminated and thus improvement in throughput is considerable. Crystals of high quality can be formed. See pages 52 and 53 of the specification as filed. See also Fig. 15 and pages 53 and 54. There are other examples throughout the specification showing the importance of the accumulation feature, all

supporting the feature that the implied structure is different from one that is processed differently.

Each of independent claims recites that a thin film semiconductor is formed by irradiating an amorphous semiconductor substrate with an energy beam that has an adjusted cross sectional shape so that a region of the substrate is irradiated with a single shot, so that a resultant polycrystalline silicon substrate is uniform in its crystallinity. Throughout the present specification (i.e., page 51, lines 7 to 12) it is repeatedly taught that by irradiating the entirety of the unit size of the thin film semiconductor device that the crystallization of the silicon film is made continuous, avoiding the formation of borders in the crystallized silicon. The specification also teaches that such borders are the product of conventional crystallization processes that involve the piecemeal irradiation of several adjacent regions of the unit size of the semiconductor device. The borders in the conventional process are the result of slight overlapping of regions that are separately irradiated. Consequently, the single shot irradiation process of the present invention does ascribe a structural limitation to the resultant thin film semiconductor that sets the structure apart from thin film semiconductors that are formed by irradiation of several adjacent regions in a unit area.

Failure to give weight to the "accumulated without exposure to air limitation" is inconsistent with the principles of sections 102 and 103 of the Patent Act because the ignored limitation is neither expressly or inherently described in a single prior art reference. "A claim is anticipated [under 35 U.S.C. § 102] only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987) (emphasis added). See M.P.E.P. § 2131. Likewise, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." M.P.E.P. § 2143.03. Accord. M.P.E.P. § 706.02(j). Because the above-discussed features of the claims are neither taught nor suggested by the prior art of record, it is respectfully submitted that the rejections of the claims cannot be sustained for failure to consider the accumulation without air exposure feature.

Accordingly, all claims are to be considered with the subject limitation in place, and are urged to be patentable over the art applied. At this juncture, a reversal of the position of the

examiner by this Board will result in a remand for consideration of the patentability of the claims over art then cited to include this missing feature.

C. Failure to Consider the "Irradiated with Pulse Light" Limitation is Error

The second full paragraph at the top of page 3 of the Final Action states, as to claim 39, that the limitation "irradiated with pulse laser light having an emission time width from upstand to downfall of at lest 50 ns" is a product by process limitation. According to the specification and the foregoing explanation, the limitation on what is the polycrystalline silicon as explained is a structural limitation and is understood in the art to be a structural limitation. The specification as filed is replete with discussions of converting amorphous silicon to polycrystalline silicon according to this radiation technique; the fact that the irradiation occurs with pulse laser light having the stated emission time width from upstand to downfall as stated in the first wherein clause of claim 39 imparts a patentable feature to the claim. For example, the discussion of Fig. 18 at pages 57 to 58 and Figs. 21A to Fig 23 at pages 65 to 69 of the specification as filed point out structural changes that result from the stated pulse characteristics. See also pages 92 and 93 of the specification as filed. Accordingly, as in the test of MPEP §2113, the structure implied by that stated limitation should be considered. See In re Garnero, supra.

D. The Failure to Consider the "Cooling" Limitation in Claim 73 is Error.

The applicable test of MPEP §2113 and In re Garnero, supra are also applicable here. The examiner argued that the limitation "substrate is cooled to a temperature lower than room temperature" is a product by process limitation. As before, however, that limitation implies a structure for the substrate that must be considered in assessing the patentability of claim 73. That structure is discussed at pages 94 et seq. of the specification as filed in terms of the conversion of the semiconductor film contained in the irradiated region to a polycrystalline material. This feature increases the probability of generation of crystal nuclei so that the number of the crystal particles contained in the semiconductor thin film having uniform crystal particle diameters can be obtained so that the thin film can be used as an active layer.

IX. CONCLUSION

In view of the foregoing reasons, Appellant submits that the final rejection of claims 11 to 12, 17 to 18, 27 to 28, 39 to 40, 53 to 54, 63, 65, and 73 to 74 is improper and should not be sustained. Therefore, a reversal of the Final Rejection of August 28, 2004, as to claims 11 to 12, 17 to 18, 27 to 28, 39 to 40, 53 to 54, 63, 65, and 73 to 74, is respectfully requested.

Dated: January 25, 2008

Respectfully submitted,

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APPENDIX A

A complete listing of all pending claims is presented.

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Currently Amended) A thin film semiconductor device comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating thin film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein said polycrystalline silicon is an irradiation converted substrate that in the prescribed region has a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter;

a thin film transistor integrated in said prescribed region through said semiconductor thin film, wherein said converted polycrystalline silicon semiconductor film has a single-shot irradiated region, and

a cross sectional shape of said energy beam is adjusted with respect to said prescribed region to consist of irradiating said prescribed region in its entirety at a time by a single shot irradiation, so that characteristics of said thin film transistor are made uniform; and

whereby said single-shot irradiated region is a borderless irradiated region; and

[wherein] wherein said semiconductor thin film is accumulated without exposing said substrate to air to accumulate said semiconductor thin film.

12. (Previously Presented) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrates comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein said polycrystalline silicon is an irradiation converted substrate that in the prescribed region has a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter;

a thin film transistor integrated in said prescribed region through said semiconductor thin film wherein said converted polycrystalline silicon semiconductor film has a single-shot irradiated region; and

a cross sectional shape of said energy beam is adjusted with respect to said prescribed region to consist of irradiating said prescribed region in its entirety at a time by a single shot irradiation, so that characteristics of said thin film transistor are made uniform; and

whereby said single-shot irradiated region is a borderless irradiated region; and

wherein said semiconductor thin film is accumulated without exposing said substrate to air to accumulate said semiconductor thin film.

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Previously Presented) A thin film semiconductor device comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a unit of said semiconductor thin film through said gate insulating thin film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter,

wherein at least one unit of the semiconductor thin film is a single-shot irradiated unit based on a cross sectional shape of said energy beam, and

a thin film transistor is integrated and formed in said at least one unit thus subjected to irradiation at a time; and

whereby said irradiated region is a borderless irradiated region; and

whereby said film is accumulated without exposing said substrate to air, to accumulate said semiconductor thin film

18. (Previously Presented) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a unit of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein said polycrystalline silicon is an irradiation converted 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter,

wherein at least one unit of the semiconductor thin film is a single-shot irradiated unit, based on a cross sectional shape of said energy beam, and

a thin film transistor is integrated and formed in said at least one unit thus subjected to irradiation at a time; and

whereby said irradiated region is a borderless irradiated region; and

wherein said film is accumulated without exposing said substrate to air, to accumulate said semiconductor thin film.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Previously Presented) A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating thin film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein in the prescribed region said polycrystalline silicon has an irradiation converted 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter, and

said semiconductor thin film is accumulated without exposing said substrate to the air; and

whereby said irradiated region is a borderless irradiated region.

28. (Previously Presented) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein said polycrystalline silicon is an irradiation converted substrate that in the prescribed region has a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter; and

said semiconductor thin film is accumulated by alternately repeating said film forming step, where each additional formed film is about 1 nm, and said irradiation step without exposing said substrate to the air; and

whereby said irradiated region is a borderless irradiated region.

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Cancelled)

35. (Cancelled)

36. (Cancelled)

37. (Cancelled)

38. (Cancelled)

39. (Previously presented) A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate irradiated with pulse laser light having an emission time width from upstand to downfall of at least 50ns, and

a desired change to said energy intensity of said laser light from upstand to downfall of said pulse is applied to said polycrystalline silicon; and

whereby said irradiated region is a borderless irradiated region; and

wherein said film forming step and said irradiating step are alternately repeated without exposing said substrate to air, to accumulate] said semiconductor thin film is accumulated without exposing said substrate to air.

40. (Previously Presented) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate irradiated with pulse laser light having an emission time width from upstand to downfall of at least 50ns,

a desired change to said energy intensity of said laser light from upstand to downfall of said pulse is applied to said polycrystalline silicon; and

whereby said irradiated region is a borderless irradiated region; and

wherein said film without exposing said substrate to air, to accumulate said semiconductor thin film.

41. (Cancelled)

42. (Cancelled)

43. (Cancelled)

44. (Cancelled)

45. (Cancelled)

46. (Cancelled)

47. (Cancelled)

48. (Cancelled)

49. (Cancelled)

50. (Cancelled)

51. (Cancelled)

52. (Cancelled)

53. (Previously Presented) A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width of at least 50ns in a non-oxidative atmosphere,

whereby said irradiated region is a borderless irradiated region; and

wherein [said film forming step and said irradiating step are alternately repeated without exposing said substrate to air, to accumulate] said semiconductor thin film is accumulated without exposing said substrate to air.

54. (Currently amended) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area

of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width of at least 50ns,

whereby said irradiated region is a borderless irradiated region; and

wherein said film is accumulated without exposing said substrate to air, to accumulate said semiconductor thin film.

55. (Cancelled)

56. (Cancelled)

57. (Cancelled)

58. (Cancelled)

59. (Cancelled)

60. (Cancelled)

61. (Cancelled)

62. (Cancelled)

63. (Previously Presented) A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width of at least 50ns when said substrate is uniformly heated;

whereby said irradiated region is a borderless irradiated region; and

wherein said semiconductor thin film is accumulated without exposing said substrate to air.

64. (Cancelled)

65. (Previously Presented) A display device comprising a pair of substrate adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width of at least 50ns when said substrate is uniformly heated,

whereby said irradiated region is a borderless irradiated region; and

wherein said semiconductor thin film is accumulated without exposing said substrate to air.

66. (Cancelled)

67. (Cancelled)

68. (Cancelled)

69. (Cancelled)

70. (Cancelled)

71. (Cancelled)

72. (Cancelled)

73. (Previously Presented) A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-

single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width of at least 50ns when said substrate is cooled to a temperature lower than room temperature,

whereby said irradiated region is a borderless irradiated region; and

wherein said film is accumulated without exposing said substrate to air, to accumulate said semiconductor thin film.

74. (Previously Presented) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrates comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width from upstand to downfall of at least 50ns when said substrate is cooled to a temperature lower than room temperature,

whereby said irradiated region is a borderless irradiated region; and

wherein said film is accumulated without exposing said substrate to air, to accumulate said semiconductor thin film.

APPENDIX B EVIDENCE APPENDIX

There is no other evidence, other than the MPEP citation and In re Garnero copies attached which will directly affect of have a bearing on the Board's Decision in this appeal.

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2113 Product-by-Process Claims [R-1] - 2100 Patentability

2113 Product-by-Process Claims [R-1]

PRODUCT-BY-PROCESS CLAIMS ARE NOT LIMITED TO THE MANIPULATIONS OF THE RECITED STEPS, ONLY THE STRUCTURE IMPLIED BY THE STEPS

"[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted) (Claim was directed to a novolac color developer. The process of making the developer was allowed. The difference between the inventive process and the prior art was the addition of metal oxide and carboxylic acid as separate ingredients instead of adding the more expensive pre-reacted metal carboxylate. The product-by-process claim was rejected because the end product, in both the prior art and the allowed process, ends up containing metal carboxylate. The fact that the metal carboxylate is not directly added, but is instead produced in-situ does not change the end product.).

>The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g., *In re Garnero*, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979) (holding "interbonded by interfusion" to limit structure of the claimed composite and noting that terms such as "welded," "intermixed," "ground in place," "press fitted," and "etched" are capable of construction as structural limitations.)<

ONCE A PRODUCT APPEARING TO BE SUBSTANTIALLY IDENTICAL IS FOUND AND A 35 U.S.C. 102/ 103 REJECTION MADE, THE BURDEN SHIFTS TO THE APPLICANT TO SHOW AN UNOBVIOUS DIFFERENCE

"The Patent Office bears a lesser burden of proof in making out a case of *prima facie* obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. *In re Fessmann,* 489

F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. *In re Marosi,* 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983) (The claims were directed to a zeolite manufactured by mixing together various inorganic materials in solution and heating the resultant gel to form a crystalline metal silicate essentially free of alkali metal. The prior art described a process of making a zeolite which, after ion exchange to remove alkali metal, appeared to be "essentially free of alkali metal." The court upheld the rejection because the applicant had not come forward with any evidence that the prior art was not "essentially free of alkali metal" and therefore a different and unobvious product.).

Ex parte Gray, 10 USPQ2d 1922 (Bd. Pat. App. & Inter. 1989) (The prior art disclosed human nerve growth factor (b-NGF) isolated from human placental tissue. The claim was directed to b-NGF produced through genetic engineering techniques. The factor produced seemed to be substantially the same whether isolated from tissue or produced through genetic engineering. While the applicant questioned the purity of the prior art factor, no concrete evidence of an unobvious difference was presented. The Board stated that the dispositive issue is whether the claimed factor exhibits any unexpected properties compared with the factor disclosed by the prior art. The Board further stated that the applicant should have made some comparison between the two factors to establish unexpected properties since the materials appeared to be identical or only slightly different.).

THE USE OF 35 U.S.C. 102/ 103 REJECTIONS FOR PRODUCT-BY-PROCESS CLAIMS HAS BEEN APPROVED BY THE COURTS

"[T]he lack of physical description in a product-by-process claim makes determination of the patentability of the claim more difficult, since in spite of the fact that the claim may recite only process limitations, it is the patentability of the product claimed and not of the recited process steps which must be established. We are therefore of the opinion that when the prior art discloses a product which reasonably appears to be either identical with or only slightly different than a product claimed in a product-by-process claim, a rejection based alternatively on either section **102** or section **103** of the statute is eminently fair and acceptable. As a practical matter, the Patent Office is not equipped to manufacture products by the myriad of processes put before it and then obtain prior art products and make physical comparisons therewith." *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972).

browse after

Last Modified: 12/28/2007 07:01:52

Go to **MPEP - Table of Contents**

APPENDIX C RELATED PROCEEDINGS APPENDIX

There are no other pending appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal, except for a prior Board decision, attached hereto, of June 30, 2004.